



FIG.1

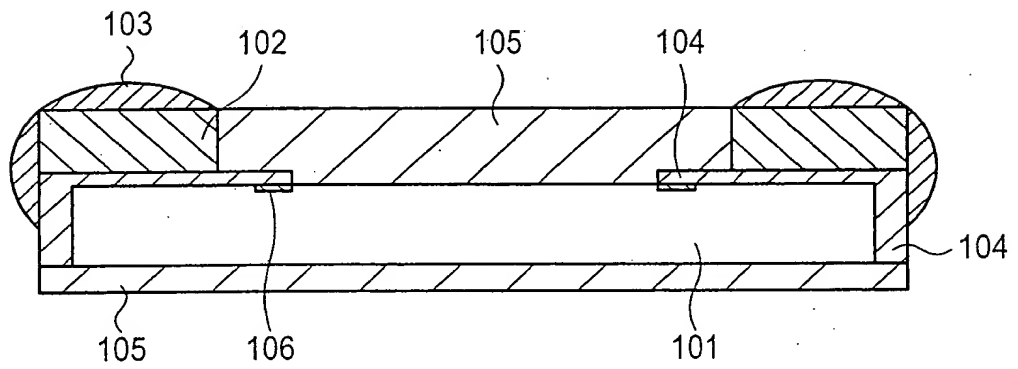


FIG.2

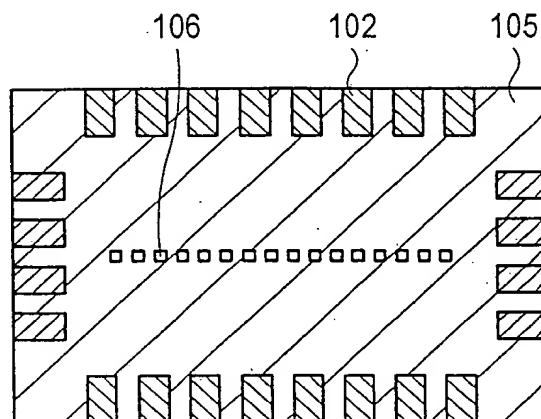


FIG.3

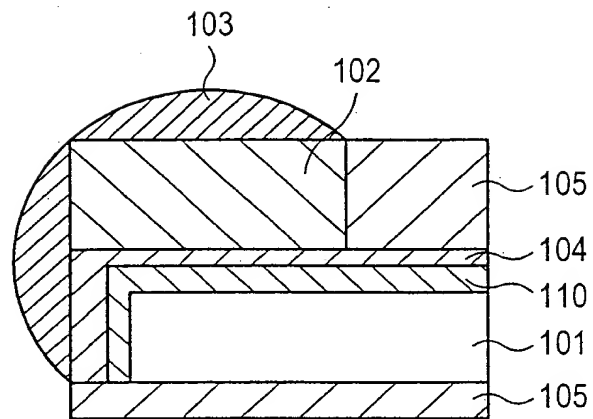


FIG.4

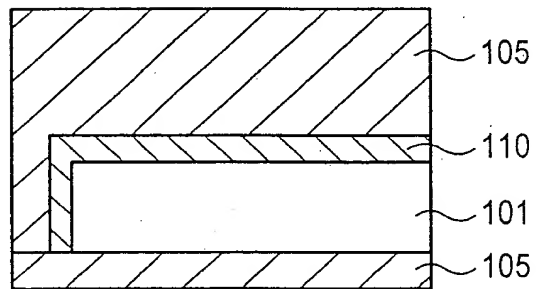


FIG.5(a)

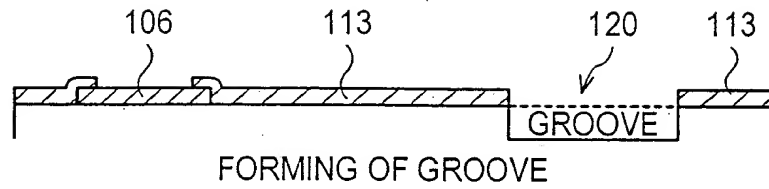


FIG.5(b)

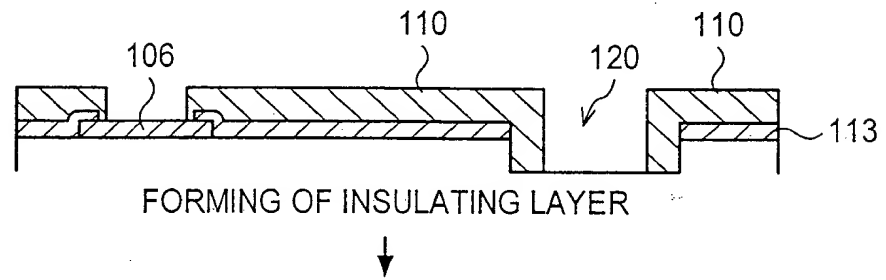


FIG.5(c)

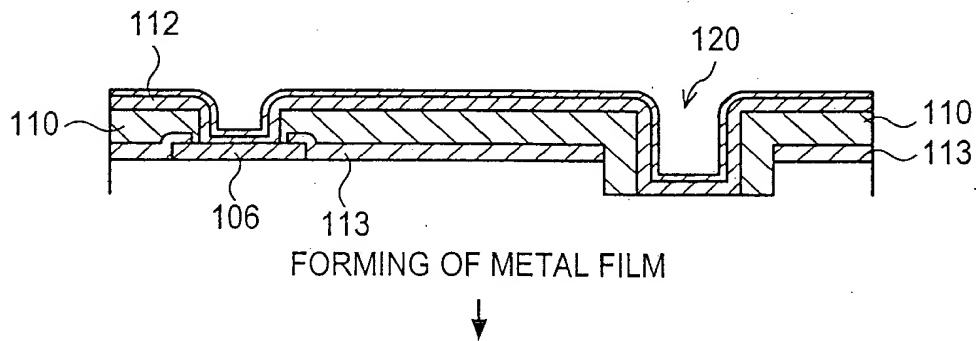
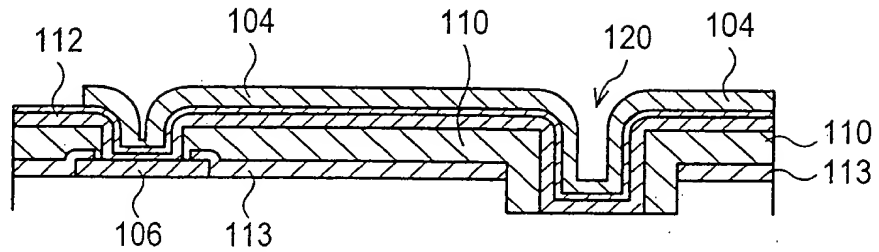


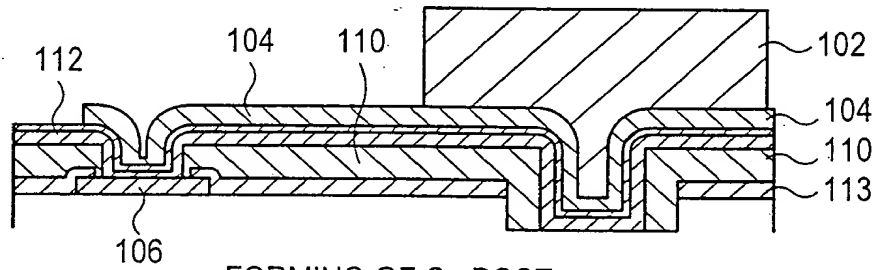
FIG.5(d)



FORMING OF RE-WIRING



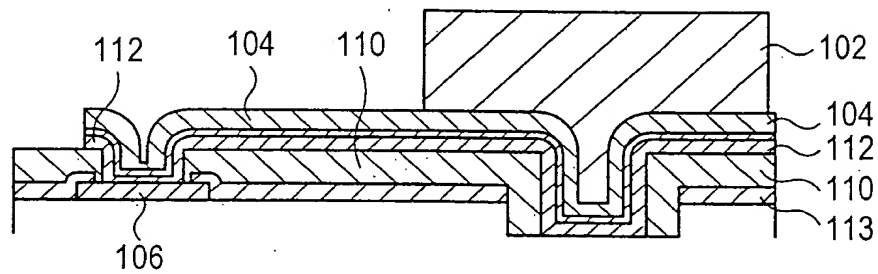
FIG.5(e)



FORMING OF Cu POST



FIG.5(f)



REMOVAL OF EXPOSED METAL FILM

FIG.6(a)

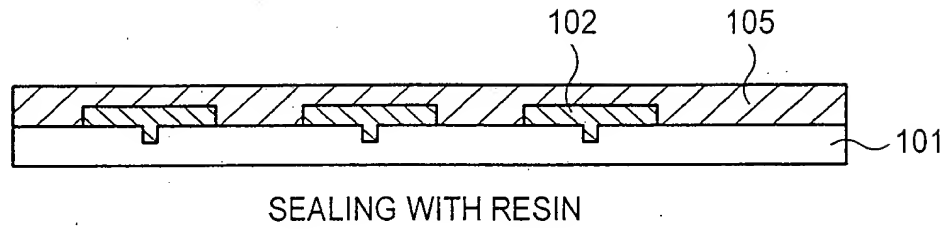


FIG.6(b)

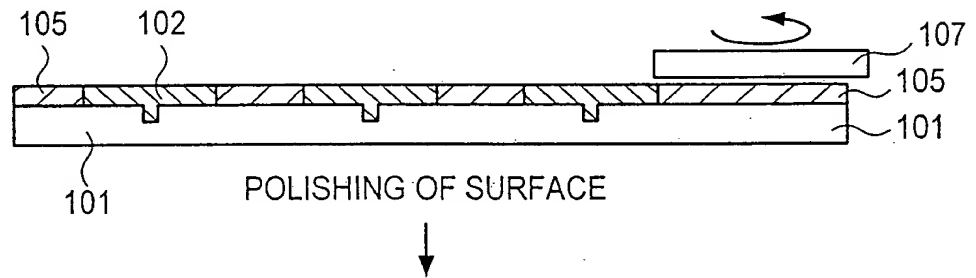


FIG.6(c)

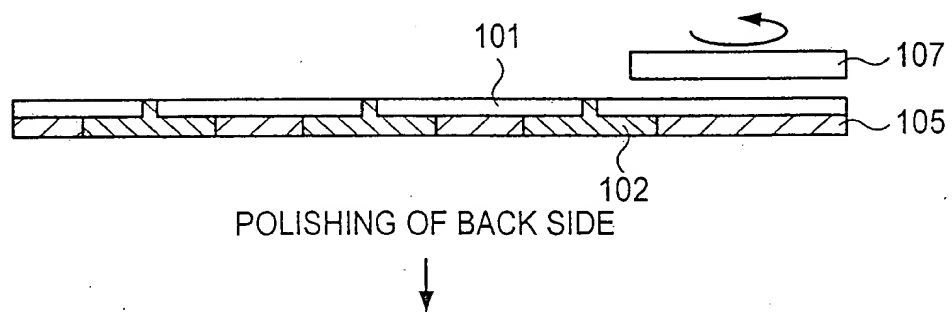


FIG.6(d)

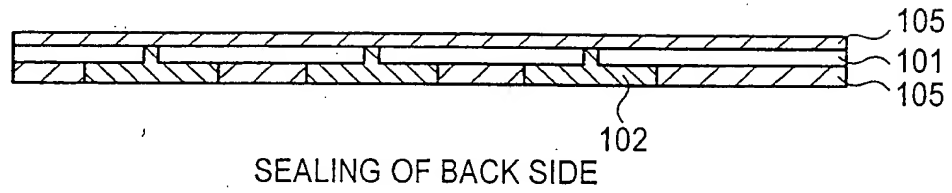


FIG.6(e)

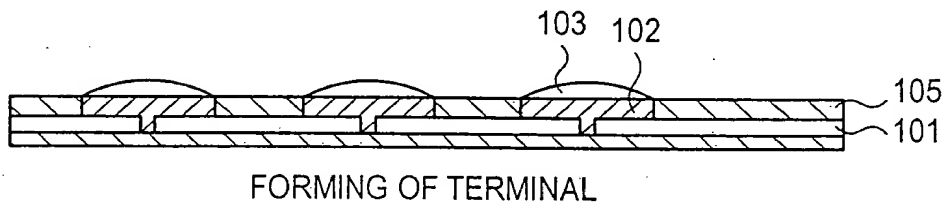


FIG.6(f)

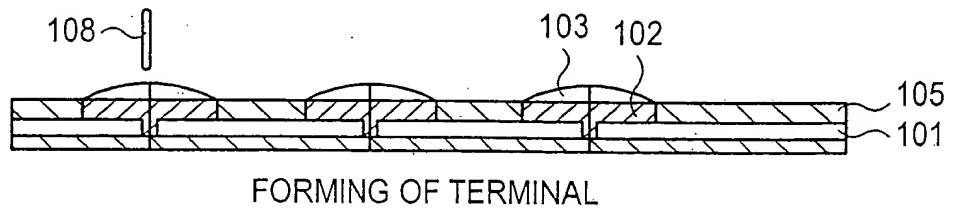


FIG.7(a)

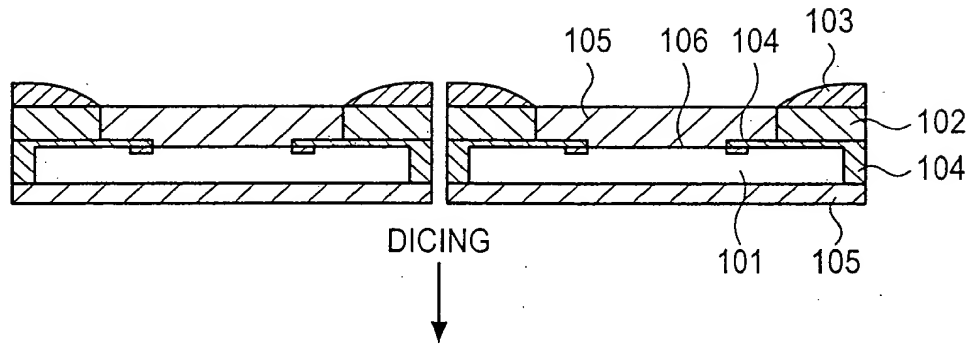


FIG.7(b)

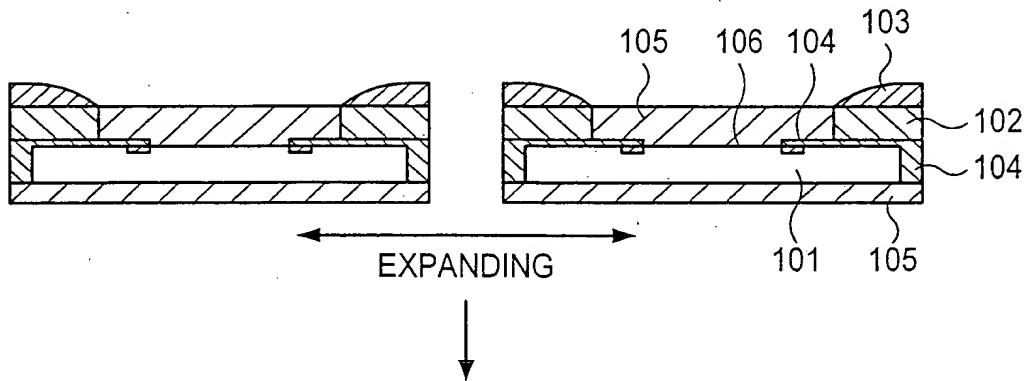


FIG.7(c)

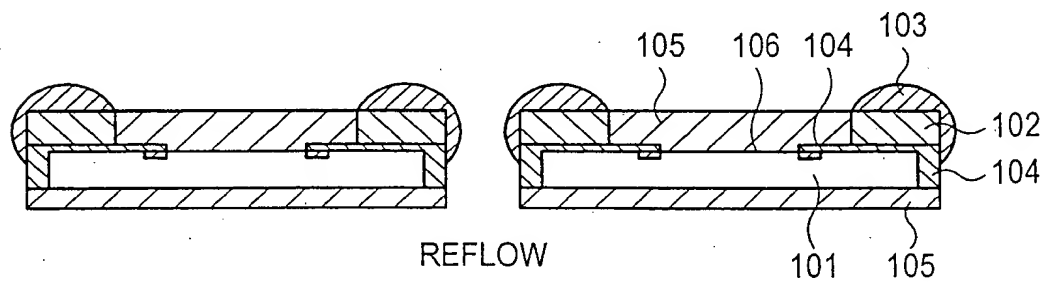


FIG.8

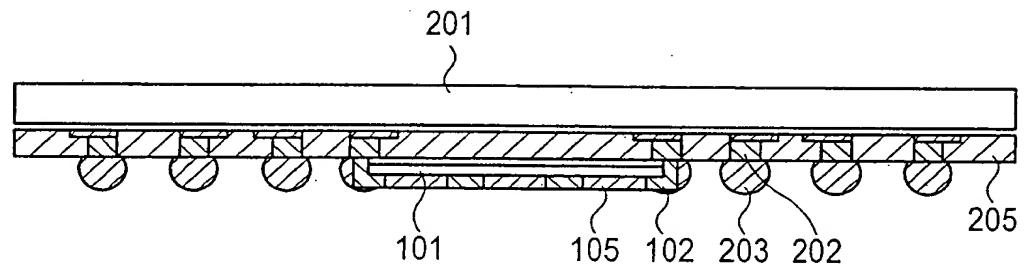


FIG.9

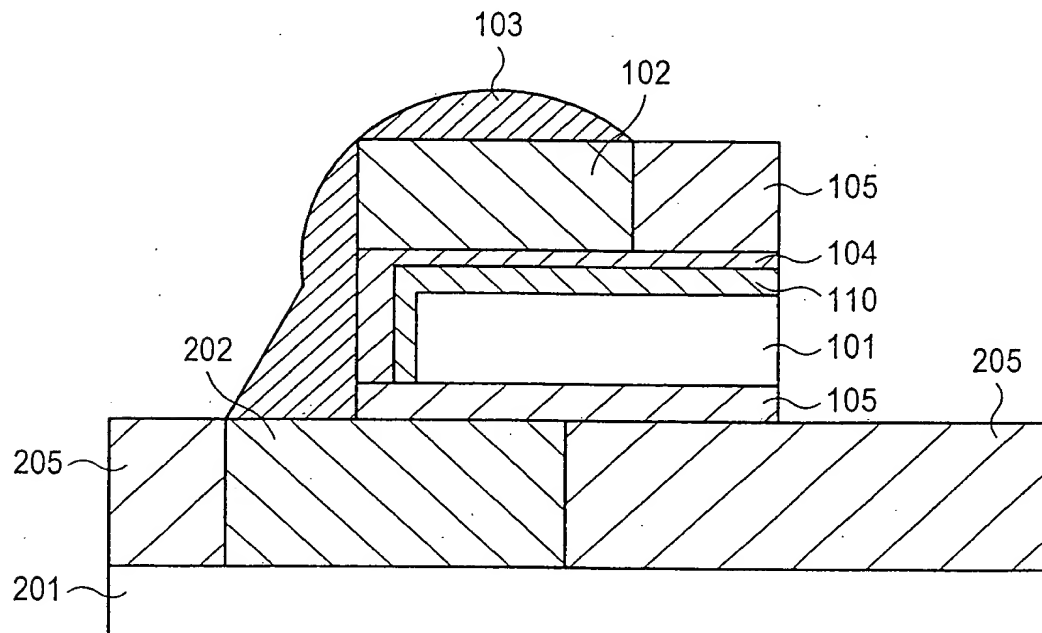


FIG.10

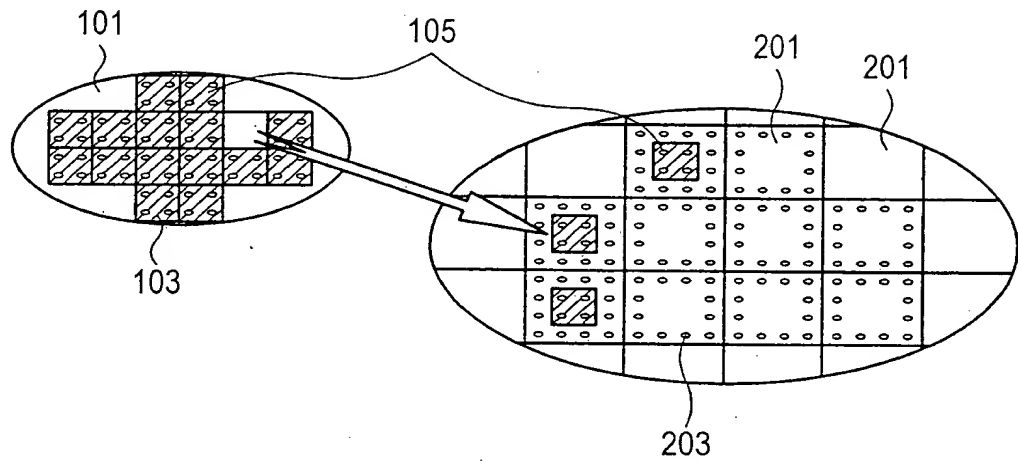


FIG.11

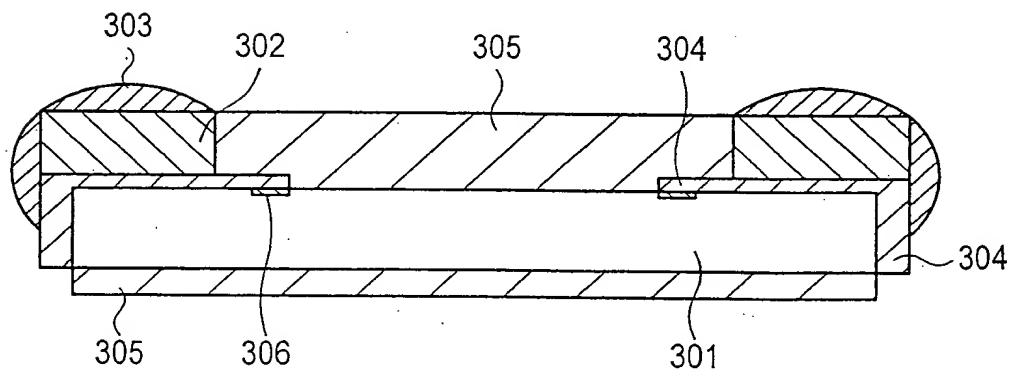


FIG.12

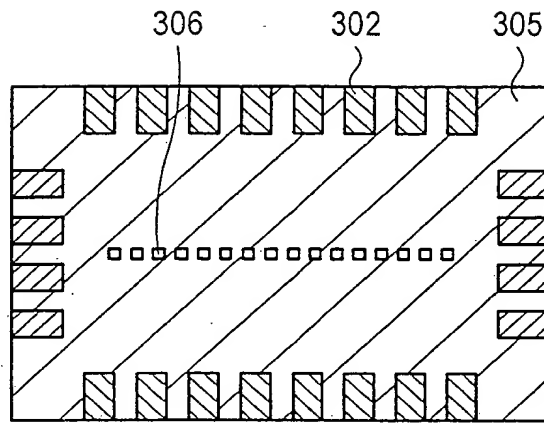


FIG.13

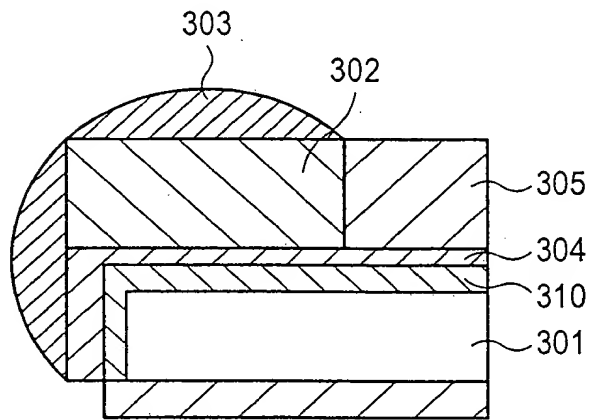


FIG.14

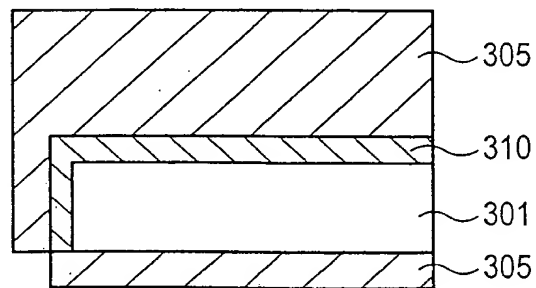
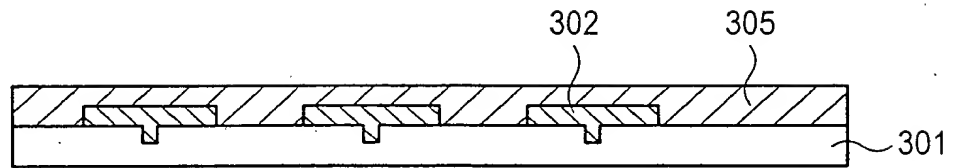


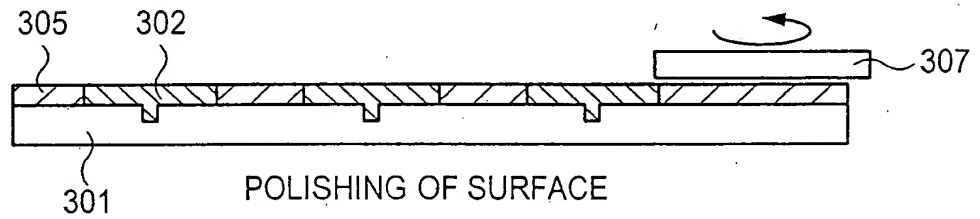
FIG.15(a)



SEALING WITH RESIN



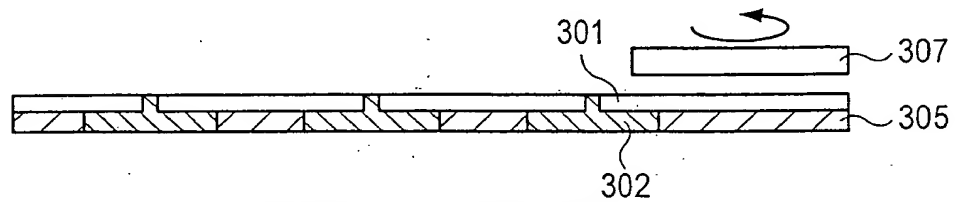
FIG.15(b)



POLISHING OF SURFACE



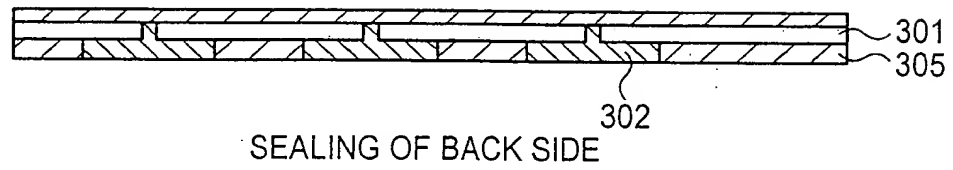
FIG.15(c)



POLISHING OF BACK SIDE



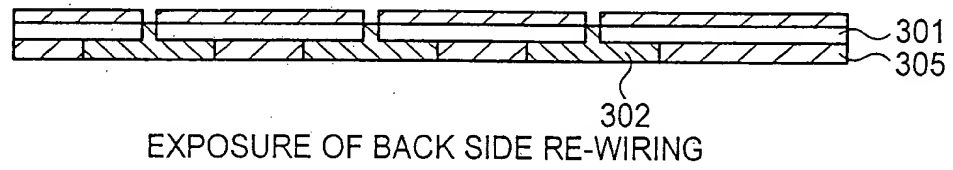
FIG.15(d)



SEALING OF BACK SIDE



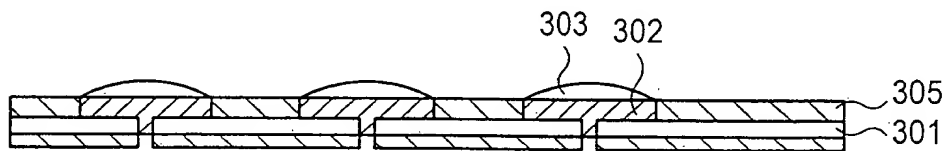
FIG.15(e)



EXPOSURE OF BACK SIDE RE-WIRING



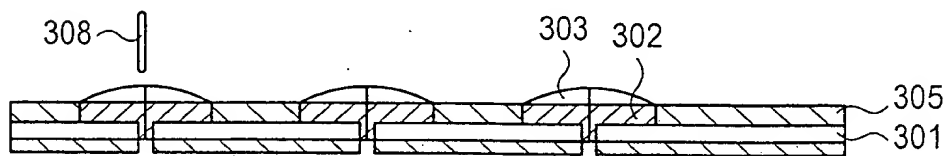
FIG.15(f)



FORMING OF TERMINAL



FIG.15(g)



FORMING OF TERMINAL

FIG.16(a)

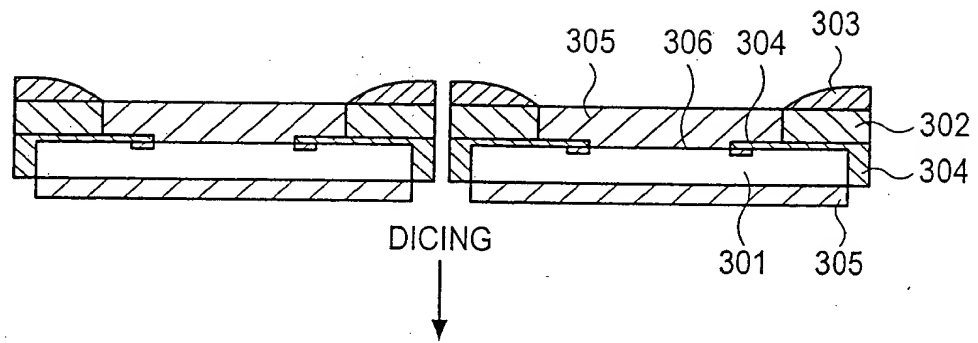


FIG.16(b)

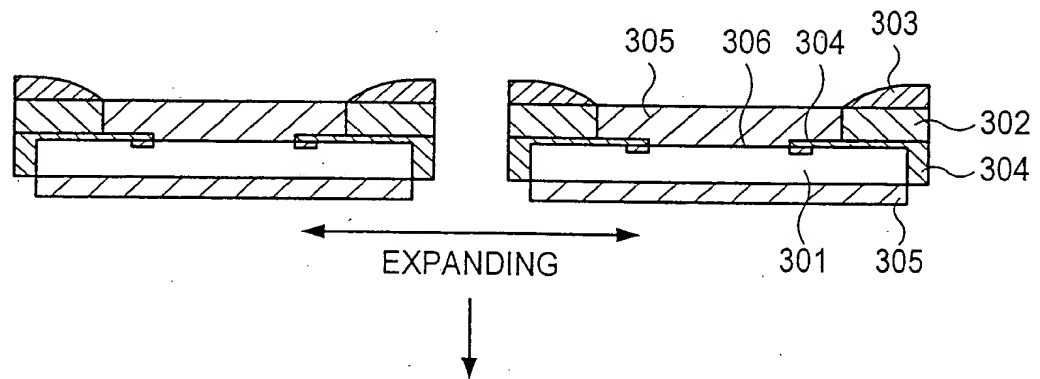


FIG.16(c)

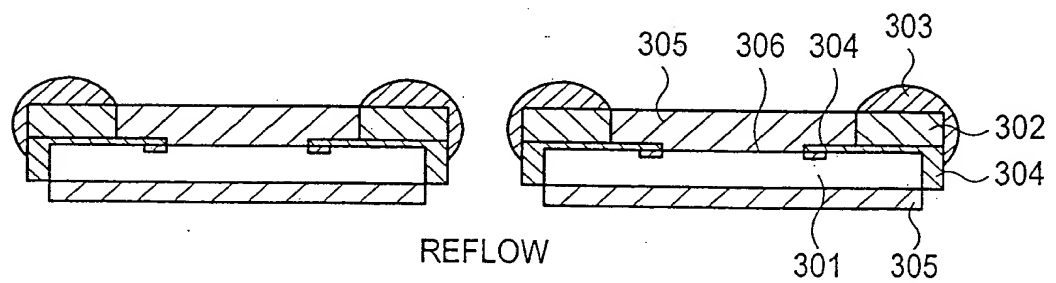


FIG.17

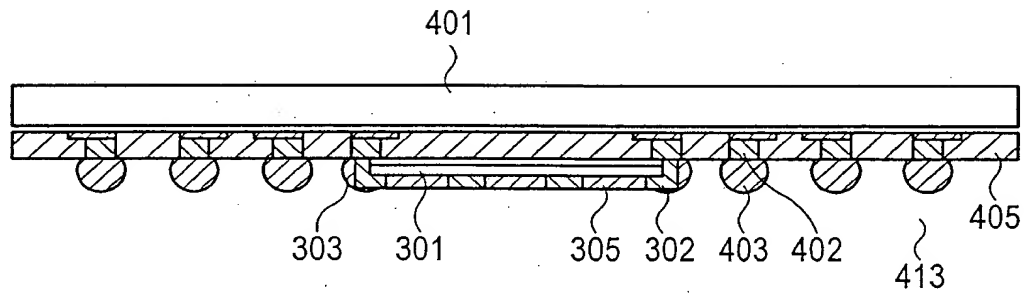


FIG.18

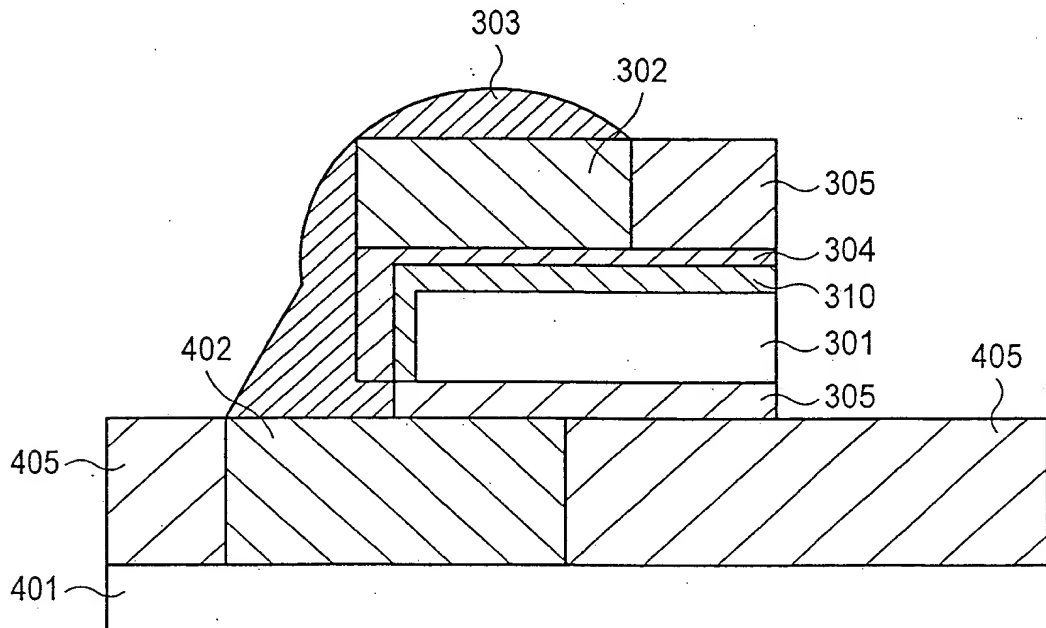


FIG.19

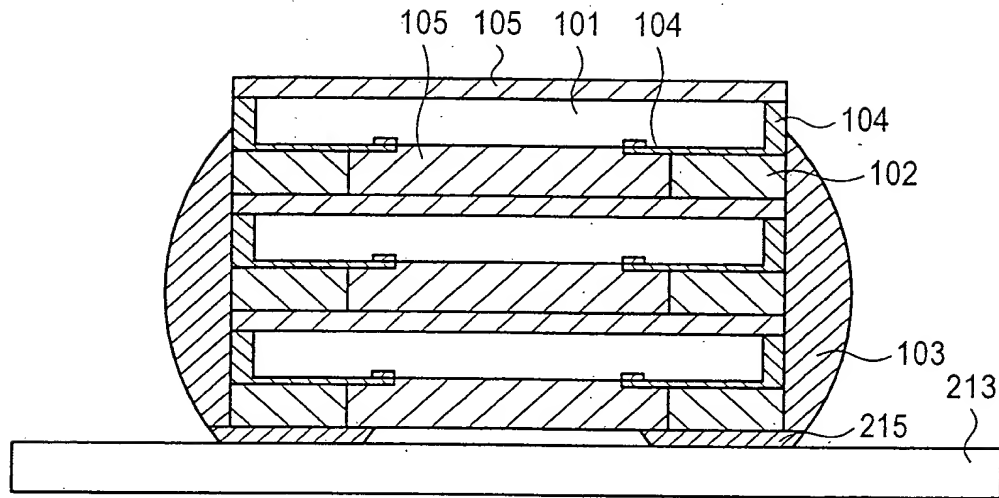


FIG.20

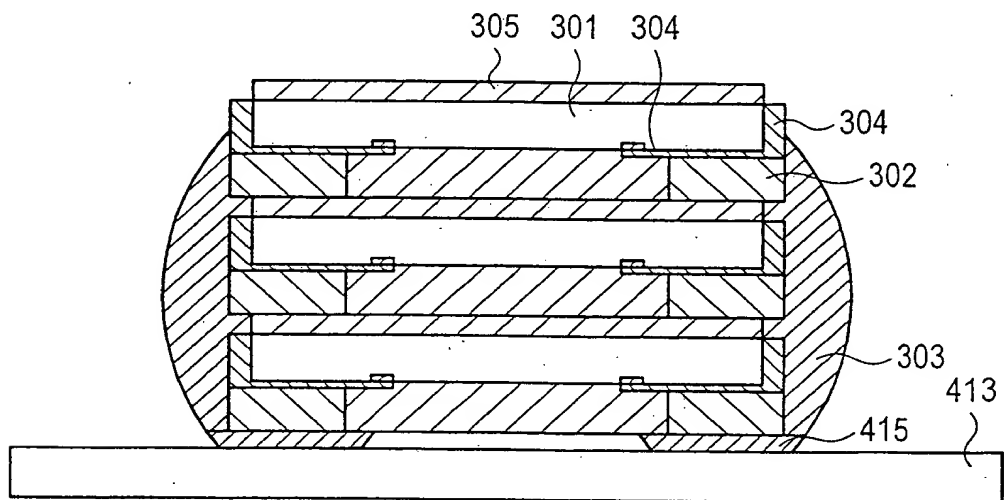


FIG.21 (Prior Art)

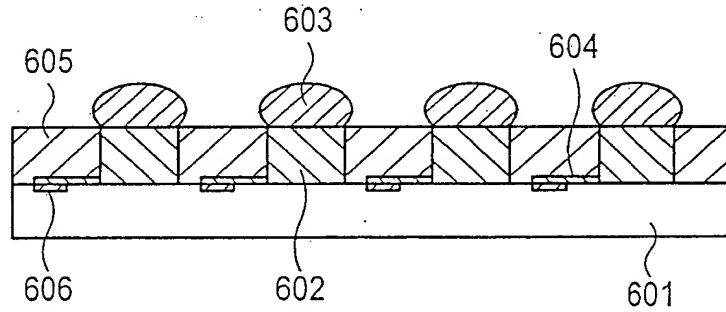


FIG.22 (Prior Art)

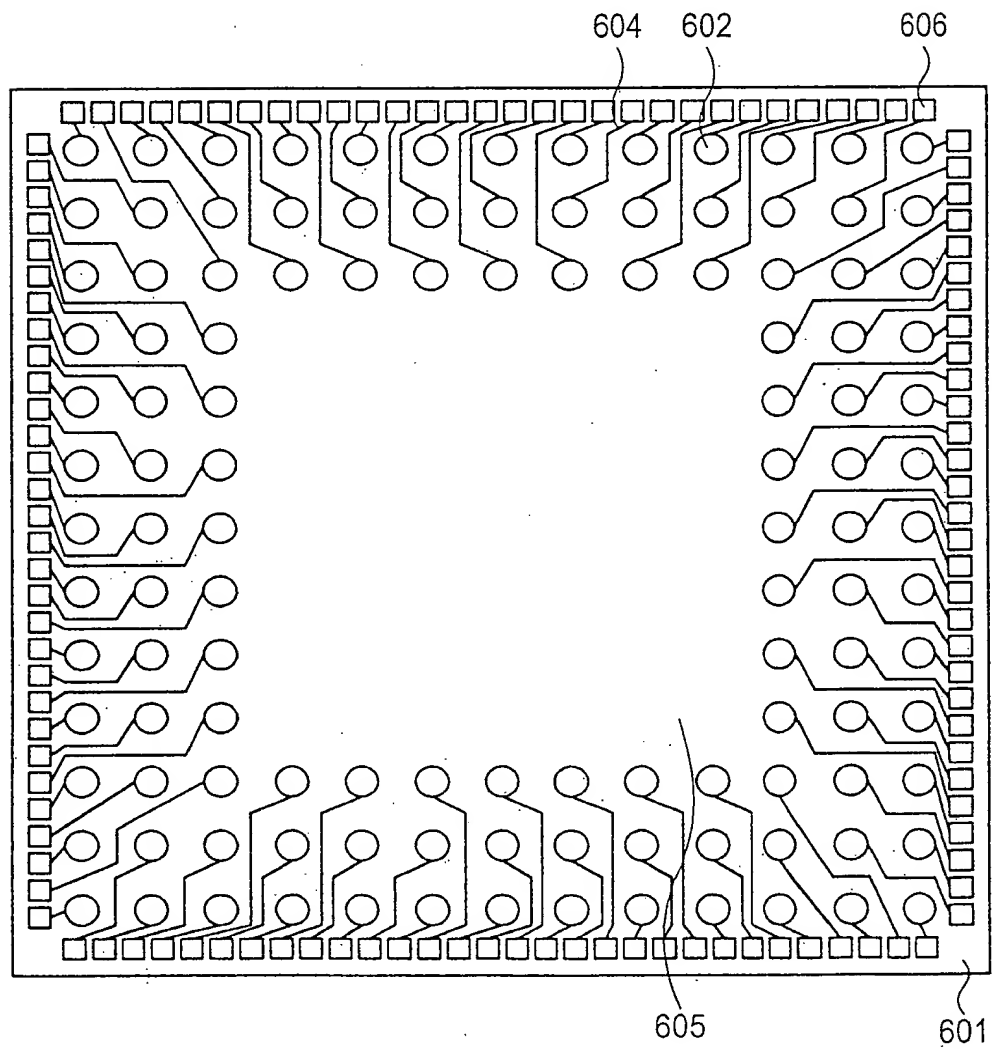


FIG.23(a) (Prior Art)

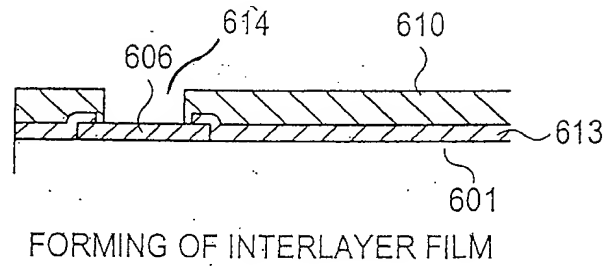


FIG.23(b) (Prior Art)

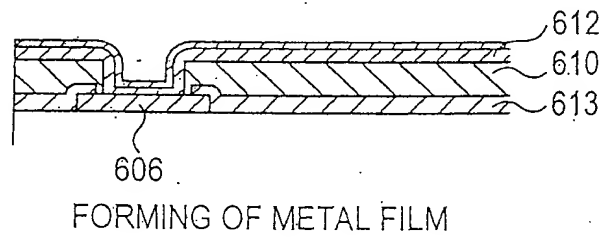
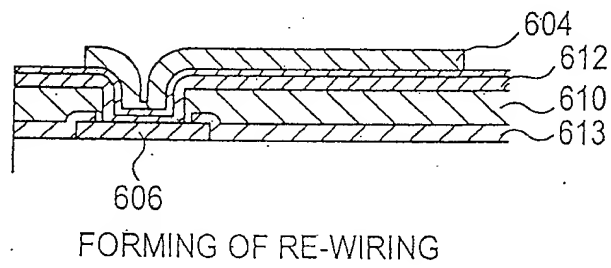


FIG.23(c) (Prior Art)



A cross-sectional view of a semiconductor device 600. The device includes a substrate 602, a first conductive layer 604, a second conductive layer 612, a third conductive layer 610, and a fourth conductive layer 613. A first conductive pad 606 is formed on the first conductive layer 604. A second conductive pad 612 is formed on the second conductive layer 612. A third conductive pad 610 is formed on the third conductive layer 610. A fourth conductive pad 613 is formed on the fourth conductive layer 613. The pads are arranged in a row, with the first conductive pad 606 being the largest and the others being smaller.

↓

Figure 6 is a cross-sectional view of a semiconductor device. The device includes a substrate with a top layer 602, a middle layer 604, and a bottom layer 612. A structure 606 is formed on the surface of the middle layer 604. A contact 604 is shown on the surface of the middle layer 604. The bottom layer 612 is further divided into layers 610 and 613.

A cross-sectional view of a substrate 601. Six solder bumps 602 are mounted on the top surface of the substrate. Each bump is represented by a rectangle with diagonal hatching.

FIG.24(b) (Prior Art)



FIG.24(c) (Prior Art)

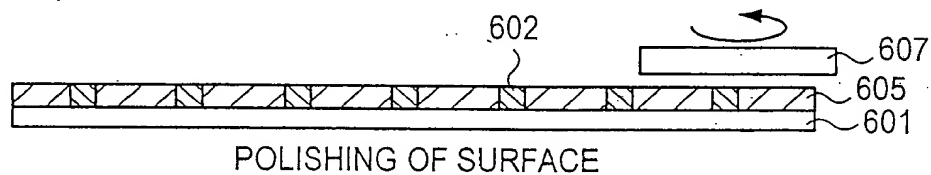


FIG.24(d) (Prior Art)

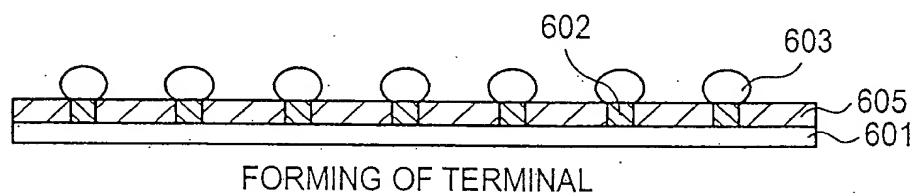
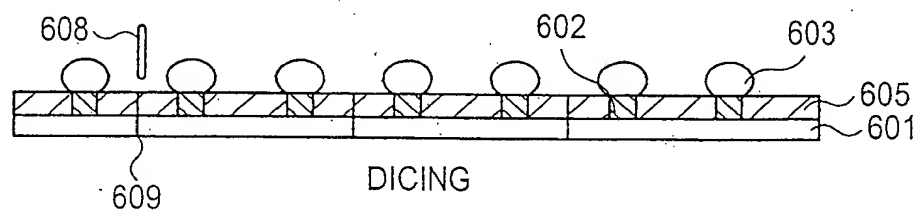


FIG.24(e) (Prior Art)



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FIG.25(a) (Prior Art)

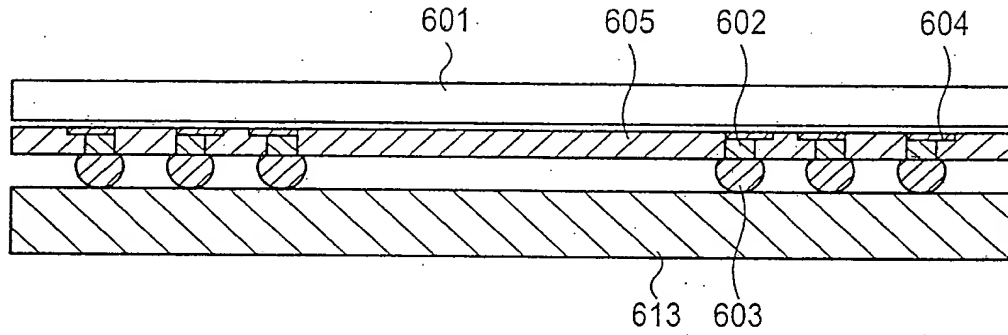


Fig. 25(b)
(Prior Art)

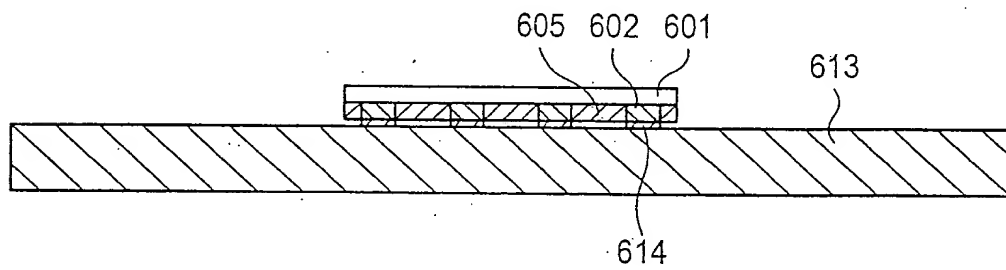


Fig. 25(c)
(Prior Art)

